WHAT IS CLAIMED IS:

1. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) , comprising:

a plurity of identical same size sub-block CAM or TCAM;

a multi-level address decoding circuits for data read and write;

a multi-level muxing of input data;

a multi-level priority encoding circuit of match address among the sub-block;

a data bus circuits to distribute the input data to every sub-block; and

a pipe line structure.

2. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein the sub-block has its own address decoding and priority encoding function.

3. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein the sub-block are equally placed in four quadruples as a matrix with number of column and rows .

4. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein the bus circuits of address and Data to write or match are routed to the mid-point at each side.

5. The bus circuits of address and Data to write or match of claim 4,wherein address and Data to write or match are sent to the center of the chip or CAM unit.

6. The bus circuits of address and Data to write or match of claim 5,wherein address and Data to write or match are sent to the right side or left side based

on the first level decoding.

7. The bus circuits of address and Data to write or match of claim 6,wherein address and Data to write or match are sent to the particular column based on the second level decoding.

8. The bus circuits of address and Data to write or match of claim 7,wherein address and Data to write or match are sent to the particular sub-block based on the third level decoding.

9. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein each sub-block is identical.

10. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein each sub-block has the same logic inter face.

11. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein the priority encoding is performed among the sub-blocks in same column.

12. A content addressable memory(CAM) unit or Ternary content addressable memory(TCAM) of claim 1, wherein the priority encoding is performed among the different column in the same quadruple.